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EXAMINER	
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ART UNIT	**PAPER NUMBER**
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/757,673	KRAVEC ET AL.	
	Examiner	Art Unit	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1,3-8,13, 37 is rejected under 35 U.S.C. 102(b) as being anticipated by Srinivasan (patent No. 6,240,485).

Srinivasan taught the invention as claimed including a data processing ("DP") system comprising (As per claims 1,6):

a) bidirectional communication bus between a first processing unit (1304) and a second (1302) and third processing unit (1306)(e.g., see fig. 13)[links 1308,1310,1312,1314,1316,1318,1320,1322,1324,1326][the CAMs receive the learn instruction and perform pattern matching processing and are therefore processors to the extent claimed];

b) Cascade system for providing bidirectional communication bus circuitry in each processing unit for bidirectional communication between the first processing unit and a second and third processing unit each adjacent to the first processing unit and within the processing units where the first processing unt is physically coupled to the second processing unit with a first link input and a first link output and to the third processing unit with a second link input and a second link output (e.g., see figs. 13,15,16).

d) Circuitry coupling the first output signal from an output of the first processing unit to the third processing unit on the second link output or selectively coupling output signal received on the first linked input from the second processing to the third processing unit on the second link (e.g., see fig. 13)[links 1308,1314,1316 coupled outputs from a first processing unit 1302 via second processing unit 1304 to processing unit 1306 also using links 1318,1324,1326 using control signals 178,138,140];

e) Circuitry for selectively coupling a third output signal received on the second link input from the third processing unit or the first output signal from the first processing to the second processing unit on the first link (e.g., see fig. 13)[signals from third processing element 1306, on links 1320,1322 are coupled via second processing unit 1304 to first processing unit 1302 also using first links 1310,1312];

f) Circuitry for coupling the third output received on the second link to an input of the first processing unit or selectively coupling the second output signal on the first link input from the second processing unit (e.g. , see fig. 13)[signal on received on second links 131320,1320 to an first input of processing unit 1302 via second processing unit 1304 or coupling output signal on first links 1310,1312 input from output of second processing unit 1304 first processing unit].

3. As to the selectively coupling, the system comprises signals (178,138,144) sent to the processing units that control the linking of the processing unit to selectively link the processors (e.g. see fig. 13). As to the enable signal in a first or second position, Srinivasan taught a cascade logic comprising(1502,1600) cascade up and cascade down logic (e.g. see figs. 15,16) that sends control signals (e.g., see col. 16, line 52-col.

17,line 22). Srinivasan also taught plural enable signals that when asserted/deasserted enable/disable the cascade transmission of data between the processing units in corresponding direction (up or down) (e.g. see col. 15, line 15-col. 16, line 67) [as understood the Srinivasan system provided enabling signals where if one processor enables input the other processors send their output to the input enabled processor. Therefore when the first processor enabled input then outputs from either the second processor or third (via the second processor in a cascade fashion) would be coupled for input. Similarly when the second processor enabled input either the first or third processor would send input to the third processor. Finally when the third processor enabled input the first processor (via the second processor in a cascade fashion) or second processor would send input to the third processor].

4. As per claim 3, Srinivasan taught blocking of communication of data between processors when the enabling signals were deasserted (e.g. see col. 15, line 15-col. 16, line 67).

5. As to the coupling limitations of claim 4,5,37 Srinvasan taught coupling of input for each of the processor to output of the other processors and coupling of outputs from each processor to inputs of the other processors (e.g., see fig. 13).

6. As per claim 7,37 Srinivasan taught function output from function logic (1502,1618,e.g., see fig. 15,16) are coupled to communication logic circuitry (134) generating a first function output signal to the first link and a first communication output signal to a first communication output.

7. As per claim 8, Srinivasan taught the second link input and the first communicatioin output are coupled to the function logic circuitry generating a second function output signal on the first link output and a second function output signal on the first function output (e.g., see fig. 13,15)[plural function outputs and communication ouputs to either processor that is coupled in cascade].

8. As per claim 13, Srinivasan taught the input of the first Processing unit is coupled to the first function output of the function logic circuit (e.g., see figs. 13,15)[the first processor is coupled to the function output of the logic in the second processor and to the function logic output of the logic within itself (first processor) .

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Srinivasan (patent No. 6,240,485) in view of Kodashiro (patent No. 5,831,997).

11. As per claim 17, Srininvasan taught first and second processing units are pattern detection processing units, each for comparing an input data byte to a pattern bye selected for a sequence of pattern bytes stored in each of first and second processing units and generating a compare output in each of the first and second processing units wherein the pattern byte in each of the processing units is selected by an address pointer(e.g. see col. 3, lines 8-64). Srinivasan did not detail storing an opcode.

Kodashiro however taught modifying a pattern in response to a compare output (selector ouput that indicates a tester model using the test pattern) and operation code stored in memory (e.g., see col. 1, lines 7-67 and col. 2, lines 25-col. 3, line 35).

12. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Srinivasan and Kodashiro. Both references were directed toward the problems determining a whether a particular pattern is stored in memory. One of ordinary skill would have been motivated to incorporate the Kodashiro teachings of generating a pattern from an instruction and test data at least to provide added applications for the system of Srinivasan as when the patterns were detected the system could modify the data for produce customized data.

13. As per claim 18,19, Srinivasan taught next address element (106). Therefore one of ordinary skill would have been motivated to increment the address using the next free address element (106) to as input to the address selector (110) (e.g., see fig. 15 of Srinivasan) These address signals are taught as input to the cam array (processor portion with the pattern data) and this would have allowed the matching to be advanced to a next pattern location (e.g., see fig. 15).

14. Claims 2,9-12,14,15,16,35,36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Srinivasan as applied to claims 1,3-8,13,37 above, and further in view of Walker (patent No. 6,127,849).

15. Claim 2, includes the limitation where the control signals for enabling input an output are present in each of the processing units including the first processing unit. This would present the situation where the signal for output from a processor and input

to the same processor came from the same processor using the same signal this would allow for simultaneous input and output to a processor. Also claim 16, claims bidirectional communication between processors are enabled by setting both first and second enable signals to logic one. Walker taught a simultaneous bidirectional I/O circuit where input an output to/from a node may occur simultaneously (e.g., see col. 4 lines 34-67) . Walker also taught Din and Dout control signals for controlling the input and output to from a node where Din and Dout are high or enabled at the same time for permitting simultaneous bidirectional input and output (e.g., see col. 9, lines 21-46). The incorporation of this feature into the Srinivasan system would have provided enable signals that could be enabled at the same time for allowing input and output to a processor simultaneously.

16. One of ordinary skill would have been motivated to combine the teachings of Srinivasan and Walker The addition of the Walker teachings of simultaneous bidirectional input and output would have allowed the combined system to more quickly transfer data for pattern matching as one processor could receive data it needed while the same processor could send data to another processor that needed data.

17. Claims 9-12,14,15,35,36 are directed to the implementation of the enabling function and communication input/output using gates and and signals. As discussed above in the discussion of the Walker and Srinivasan references in the implementation as simultaneous bidirectional transmission of signals to/from processors plural control signals were used simultaneously where both could be enabled at the same time for simultaneous bidirectional transfer. The use of gates for implementation of the logic for

enabling transmission of signals was well known in the art at the time of the claimed invention. Therefore one of ordinary skill would have been motivated to use the use of AND gates or OR gates and use the gates in combination with the systems signals to generate communication output signals and function signals such as taught by Srinivasan (e.g., see figs. 3a,5,6,8 of Walker)[walker taught the use gates in combination with signals to enable inputs and output].

18. Claims 20-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Srinivasan (patent No. 6,240,485) in view of Sceiza (patent No. 5,787,200).

19. Srinivasan taught the invention substantially as claimed including a data processing system comprising(as per claim 20):

a) Bidirectional communication bus between a first processing unit (1304) and a second (1302) and third processing unit (1306)(e.g., see fig. 13)[links 1308,1310,1312,1314,1316,1318,1320,1322,1324,1326][the CAMs receive the learn instruction and perform pattern matching processing and are therefore processors to the extent claimed];

b) Cascade system for providing bidirectional communication bus circuitry in each processing unit for bidirectional communication between the first processing unit and a second and third processing unit each adjacent to the first processing unit and within the processing units where the first processing unt is physically coupled to the second processing unit with a first link input and a first link output and to the third processing unit with a second link input and a second link output (e.g., see figs. 13,15,16).

d) Circuitry coupling the first output signal from an output of the first processing unit to the third processing unit on the second link output or selectively coupling output signal received on the first linked input from the second processing to the third processing unit on the second link (e.g., see fig. 13)[links 1308,1314,1316 coupled ouputs from a first processing unit 1302 via second processing unit 1304 to processing unit 1306 also using links 1318,1324,1326 using control signals 178,138,140];

e) Circuitry for selectively coupling a third output signal received on the second link input from the third processing unit or the first output signal from the first processing to the second processing unit on the first link (e.g., see fig. 13)[signals from third processing element 1306, on links 1320,1322 are coupled via second processing unit 1304 to first processing unit 1302 also using first links 1310,1312];

f) Circuitry for coupling the third output received on the second link to an input of the first processing unit or selectively coupling the second output signal on the first link input from the second processing unit (e.g. , see fig. 13)[signal on received on second links 131320,1320 to an first input of processing unit 1302 via second processing unit 1304 or coupling output signal on first links 1310,1312 input from output of second processing unit 1304 first processing unit].

20. As to the selectively coupling, the system comprises signals (178,138,144) sent to the processing units that control the linking of the processing unit to selectively link the processors (e.g. see fig. 13). As to the enable signal in a first or second position, Srinivasan taught a cascade logic comprising(1502,1600) cascade up and cascade down logic (e.g. see figs. 15,16) that sends control signals (e.g., see col. 16, line 52-col.

17,line 22). Srinivasan also taught plural enable signals that when asserted/deasserted enable/disable the cascade transmission of data between the processing units in corresponding direction (up or down) (e.g. see col. 15, line 15-col. 16, line 67) [as understood the Srinivasan system provided enabling signals where if one processor enables input the other processors send their output to the input enabled processor. Therefore when the first processor enabled input then outputs from either the second processor or third (via the second processor in a cascade fashion) would be coupled for input. Similarly when the second processor enabled input either the first or third processor would send input to the third processor. Finally when the third processor enabled input the first processor (via the second processor in a cascade fashion) or second processor would send input to the third processor].

21. Srinivasan did not expressly detail a central processing unit (claim 20). Sceiza however taught a charater pattern reconition system comprising a central processor (master processor), RAM (external memory 5). As to the pattern detection engines Srinivasan taught processing unit (CAMs that processing LEARN instructions) for detecting patterns (as detailed above).

22. It would have been obvious to one of ordinary skill to combine the teachings of Srinivasan and Sceiza. Both references were directed toward the problems of recognizing patterns stored in memory. The addition of the Sceiza teachings of a master processor and external memory would have provided the Srinivasan a means to receive control commands and data and a place to store output data.

23. As per claim 21, Srinivasan taught function output from function logic (1502,1618,e.g., see fig. 15,16) are coupled to communication logic circuitry (134) generating a first function output signal to the first link and a first communication output signal to a first communication output.

24. As per claim 22, Srinivasan taught the second link input and the first communicatioin output are coupled to the function logic circuitry generating a second function output signal on the first link output and a second function output signal on the first function output (e.g., see fig. 13,15)[plural function outputs and communication ouputs to either processor that is coupled in cascade].

25. As per claim 27, Srinivasan taught the input of the first Processing unit is coupled to the first function output of the function logic circuit (e.g., see figs. 13,15)[the first processor is coupled to the function output of the logic in the second processor and to the function logic output of the logic within itself (first processor) .

26. Claims 23-26,28,29 these claims are directed to the implementation of the enabling function and communication input/output using gates and and signals. As discussed above in the discussion of the Walker and Srinivasan references in the implementation as simultaneous bidirectional transmission of signals to/from processors plural control signals were used simultaneously where both could be enabled at the same time for simultaneous bidirectional transfer. The use of gates for implementation of the logic for enabling transmission of signals was well known in the art at the time of the claimed invention. Therefore one of ordinary skill would have been motivated to use the use of AND gates or OR gates and use the gates in combination with the systems

signals to generate communication output signals and function signals such as taught by Srinivasan (e.g., see figs. 3a,5,6,8 of Walker)[Walker taught the use gates in combination with signals to enable inputs and output].

27. Claims 31-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Srinivasan (patent No. 6,240,485) in view of Sceiza (patent No. 5,787,200)as applied to claims 20-29 above and further in view of Kodashiro (patent No. 5,831,997).

28. As per claim 31, Srininvasan taught first and second processing units are pattern detection processing units, each for comparing an input data byte to a pattern bye selected for a sequence of pattern bytes stored in each of first and second processing units and generating a compare output in each of the first and second processing units wherein the pattern byte in each of the processing units is selected by an address pointer(e.g. see col. 3, lines 8-64). Srinivasan did not detail storing an opcode. Kodashiro however taught modifying a pattern in response to a compare output (selector ouput that indicates a tester model using the test pattern) and operation code stored in memory (e.g., see col. 1, lines 7-67 and col. 2, lines 25-col. 3, line 35).

29. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Srinivasan and Kodashiro. Both references were directed toward the problems determining a whether a particular pattern is stored in memory. One of ordinary skill would have been motivated to incorporate the Kodashiro teachings of generating a pattern from an instruction and test data at least to provide added applications for the system of Srinivasan as when the patterns were detected the system could modify the data for produce customized data.

30. As per claim 32,33 Srinivasan taught next address element (106). Therefore one of ordinary skill would have been motivated to increment the address using the next free address element (106) to as input to the address selector (110) (e.g., see fig. 15 of Srinivasan) These address signals are taught as input to the cam arry (processor portion with the pattern data) and this would have allowed the matching to be advanced to a next pattern location (e.g., see fig. 15).

31. Claims 30 rejected under 35 U.S.C. 103(a) as being unpatentable over Srinivasan in view of Sceiza (patent No. 5,787,200).as applied to claims 20-29 above, and further in view of Walker (patent No. 6,127,849).

32. Claim 30 includes the limitation where the control signals for enabling input an output are present in each of the processing units including the first processing unit. This would present the situation where the signal for output from a processor and input to the same processor came from the same processor using the same signal this would allow for simultaneous input and output to a processor. Walker taught a simultaneous bidirectional I/O circuit where input an output to/from a node may occur simultaneously (e.g., see col. 4 lines 34-67) . Walker also taught Din and Dout control signals for controlling the input and output to from a node where Din and Dout are high or enabled at the same time for permitting simultaneous bidirectional input and output (e.g., see col. 9, lines 21-46). The incorporation of this feature into the Srinivasan system would have provided enable signals that could be enabled at the same time for allowing input and output to a processor simultaneously.

33. One of ordinary skill would have been motivated to combine the teachings of Srinivasan and Walker the addition of the Walker teachings of simultaneous bidirectional input and output would have allowed the combined system to more quickly transfer data for pattern matching as one processor could receive data it needed while the same processor could send data to another processor that needed data.

34. Claim 30 is are directed to the implementation of the enabling function and communication input/output using gates and signals. As discussed above in the discussion of the Walker and Srinivasan references in the implementation as simultaneous bidirectional transmission of signals to/from processors plural control signals were used simultaneously where both could be enabled at the same time for simultaneous bidirectional transfer. The use of gates for implementation of the logic for enabling transmission of signals was well known in the art at the time of the claimed invention. Therefore one of ordinary skill would have been motivated to use the use of AND gates or OR gates and use the gates in combination with the systems signals to generate communication output signals and function signals such as taught by Srinivasan (e.g., see figs. 3a,5,6,8 of Walker)[Walker taught the use gates in combination with signals to enable inputs and output].

35. Claims 34 is rejected under 35 U.S.C. 103(a) as being unpatentable over Srinivasan in view of Walker (patent No. 6,127,849).

36. Srinvasan taught the invention substantially as claimed including a data processing ("DP") system comprising (As per claim 34):

a) Bidirectional communication bus between a first processing unit (1304) and a second (1302) and third processing (1306)(e.g., see fig. 13)[links 1308,1310,1312,1314,1316,1318,1320,1322,1324,1326][the CAMs receive the learn instruction and perform pattern matching processing and are therefore processors to the extent claimed];

b) Cascade system for providing bidirectional communication bus circuitry in each processing unit for bidirectional communication between the first processing unit and a second and third processing unit each adjacent to the first processing unit and within the processing units where the first processing unit is physically coupled to the second processing unit with a first link input and a first link output and to the third processing unit with a second link input and a second link output (e.g., see figs 13,15,16).

d) Circuitry coupling the first output signal from an output of the first processing unit to the third processing unit on the second link output or selectively coupling output signal received on the first linked input from the second processing to the third processing unit on the second link (e.g., see fig. 13)[links 1308,1314,1316 coupled ouputs from a first processing unit 1302 via second processing unit 1304 to processing unit 1306 also using links 1318,1324,1326 using control signals 178,138,140]

e) Circuitry for selectively coupling a third output signal received on the second link input from the third processing unit or the first output signal from the first processing to the second processing unit on the first link (e.g., see fig. 13)[signals from third

processing element 1306, on links 1320,1322 are coupled via second processing unit 1304 to first processing unit 1302 also using first links 1310,1312].

f) Circuitry for coupling the third output received on the second link to an input of the first processing unit or selectively coupling the second output signal on the first link input from the second processing unit (e.g. , see fig. 13)[signal on received on second links 131320,1320 to an first input of processing unit 1302 via second processing unit 1304 or coupling output signal on first links 1310,1312 input from output of second processing unit 1304 first processing unit].

37. As to the selectively coupling the system comprises signals (178,138,144) sent to the processing units that control the linking of the processing unit to selectively link the processors (e.g. see fig. 13). As to the enable signal in a first or second position Srinivasan taught a cascade logic comprising(1502,1600)comprising cascade up and cascade down logic (e.g. see figs. 15,16) that sends control signals (e.g., see col. 16, lines 52-col. 17,line 22). Srinivasan also taught plural enable signals that when asserted/deasserted enable/disable the cascade transmission of data between the processing units in corresponding direction (up or down) (e.g. see col. 15, line 15-col. 16, line 67) [as understood the Srinivasan system provided enabling signals where if one processor enables input the other processors send their output to the input enabled processor. Therefore when the first processor enabled input then outputs from either the second processor or third (via the second processor in a cascade fashion) would be coupled for input. Similarly when the second processor enabled input either the first or third processor would send input to the third processor. Finally when the third processor

enabled input the first processor (via the second processor in a cascade fashion) or second processor would send input to the third processor]. Walker taught a simultaneous bidirectional I/O circuit where input an output to/from a node may occur simultaneously (e.g., see col. 4 lines 34-67) . Walker also taught Din and Dout control signals for controlling the input and output to from a node where Din and Dout are high or enabled at the same time for permitting simultaneous bidirectional input and output (e.g., see col. 9, lines 21-46). The incorporation of this feature into the Srinivasan system would have provided enable signals that could be enabled at the same time for allowing input and output to a processor simultaneously.

38. Claim 34 is directed to the implementation of the function and communication input/output using gates and signals. As discussed above in the discussion of the Walker and Srinivasan references in the implementation as simultaneous bidirectional transmission of signals to/from processors plural control signals were used simultaneously where both could be enabled at the same time for simultaneous bidirectional transfer. The use of gates for implementation of the logic for enabling transmission of signals was well known in the art at the time of the claimed invention. Therefore one of ordinary skill would have been motivated to use the use of AND gates or OR gates and use the gates in combination with the systems signals to generate communication output signals and function signals such as taught by Srinivasan (e.g., see figs. 3a,5,6,8 of Walker)[walker taught the use gates in combination with signals to enable inputs and output].

39. One of ordinary skill would have been motivated to combine the teachings of Srinivasan and Walker the addition of the Walker teachings of simultaneous bidirectional input and output would have allowed the combined system to more quickly transfer data for pattern matching as one processor could receive data it needed while the same processor could send data to another processor that needed data.

40. Claims 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Srinivasan (patent No. 6,240,485) as applied to claim 6 above and further in view of Kodashiro (patent No. 5,831,997).

41. As per claim 38, Srinivasan taught first and second processing units are pattern detection processing units, each for comparing an input data byte to a pattern bye selected for a sequence of pattern bytes stored in each of first and second processing units and generating a compare output in each of the first and second processing units wherein the pattern byte in each of the processing units is selected by an address pointer(e.g. see col. 3, lines 8-64). Srinivasan did not detail storing an opcode. Kodashiro however taught modifying a pattern in response to a compare output (selector ouput that indicates a tester model using the test pattern) and operation code stored in memory (e.g., see col. 1, lines 7-67 and col. 2, lines 25-col. 3, line 35).

42. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Srinivasan and Kodashiro. Both references were directed toward the problems determining a whether a particular pattern is stored in memory. One of ordinary skill would have been motivated to incorporate the Kodashiro teachings of generating a pattern from an instruction and test data at least to provide added

applications for the system of Srinivasan as when the patterns were detected the system could modify the data for produce customized data.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kemeny (patent No. 5,548,773) disclosed a digital parallel processor array (e.g see abstract).

Wyland (patent No. 5,440,715) disclosed a system for expanding the width of a content addressable memory (e.g., see abstract).

Houseman (patent No. 4,559,618) disclosed a content addressable module with associative cells (e.g. see abstract).

Kumagai (patent No. 6,847,346) disclosed a semiconductor device equipped with transfer circuit for cascade connection (e.g., see abstract).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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